In the Specification

The paragraph beginning at line 12 on page 15 and extending through line 19 on page 15 has been amended as follows:

Referring to Fig. 21, wafer fragment 10b is exposed to subsequent processing analogous to the prior art processing described above with reference to Figs. 6-12 to form isolation regions 58 and a polysilicon layer 38 overlying isolation regions 58. As shown, steps 52 define an outer lateral periphery of isolation regions 58. Such outer periphery is further outward than an outer periphery 33 of isolation regions 30 of Fig. 12. Such has resulted in the alleviation (shown as elimination) of dips 32 (Fig. 12) of the prior art isolation regions. Isolation regions 58 include first and second curved segments, 82 and 84, respectively.